CLAIMS

What is claimed is.

1. A process of forming a phase-change memory comprising:

providing a phase-change memory cell substrate including a lower electrode in a first dielectric film, wherein the lower electrode comprises an upper section and a lower section;

removing a portion of the first dielectric film to cause the upper section to form a prominence; and

increasing resistivity in the upper section.

2. The process according to claim 1, further comprising:

forming a second dielectric film over the upper section; and

removing a portion of the second dielectric film to expose an upper surface of the upper section.

3. The process according to claim 1, further comprising:

forming a second dielectric film over the upper section, wherein the second dielectric film is patterned over the upper section; and

removing a portion of the second dielectric film to expose an upper surface of the upper section.

4. The process according to claim 3, wherein removing is carried out by a spacer etch process.

5. The process according to claim 1, wherein removing further comprises:

performing a spacer etch upon the second dielectric film under conditions sufficient to remove dielectric material formed from the upper section during increasing resistivity.

6. The process according to claim 3, wherein removing is carried out by a mechanical planarization process.

7. The process according to claim 1, wherein increasing resistivity further comprises:

thermally treating the upper section under conditions to form at least a dielectric husk thereon.

8. The process according to claim 1, wherein increasing resistivity further comprises:

thermally treating the upper section under conditions to form at least a conductivity gradient taken from a lateral surface of the upper section and tending toward a symmetry line thereof.

9. The process according to claim 1, wherein increasing resistivity further comprises:

performing an etch on the upper section.

10. The process according to claim 1, wherein increasing resistivity further comprises:

performing an isotropic etch on the upper section.

11. The process according to claim 1, wherein increasing resistivity further comprises:

performing a facet etch on the upper section.

12. The process according to claim 1, wherein providing a phase-change memory cell substrate including a lower electrode further comprises:

forming a metal compound film in a recess.

13. The process according to claim 1, wherein providing a phase-change memory cell substrate including a lower electrode further comprises:

forming a refractory metal compound film in a recess.

14. The process according to claim 1, wherein providing a phase-change memory cell substrate including a lower electrode further comprises:

forming a refractory metal compound film in a recess, wherein the refractory metal compound film is selected from tantalum nitride, titanium nitride, tungsten nitride, tanatalum silicon nitride, titanium silicon nitride, and tungsten silicon nitride.

15. The process according to claim 1, wherein providing a phase-change memory cell substrate including a lower electrode further comprises:

forming a polysilicon film in a recess.

16. The process according to claim 1, further comprising:

forming a phase-change material over the upper section.

17. The process according to claim 1, wherein increasing resistivity further comprises:

forming a high resistivity film over the upper section; and

heating the high resistivity film and the upper section in an oxidizing atmosphere.

18. A phase-change memory cell comprising

phase-change memory cell substrate including a lower electrode in a first dielectric film, wherein the lower electrode comprises an upper section and a lower section;

wherein the upper section forms a prominence that extends out of the first dielectric film; and

wherein the upper section has a greater resistivity than the lower section.

19. The phase-change memory cell according to claim 18, further comprising:

a second dielectric film disposed against the upper section, wherein the second dielectric film to exposes an upper surface of the upper section.

20. The phase-change memory cell according to claim 18, further comprising:

a second dielectric film disposed against the upper section, wherein the second dielectric film to exposes an upper surface of the upper section, wherein the second dielectric film has a blanket configuration.

21. The phase-change memory cell according to claim 18, wherein the upper section has a dielectric husk disposed thereon.

22. The phase-change memory cell according to claim 18, wherein the upper section forms at least a conductivity gradient taken from a lateral surface of the upper section and tending toward a symmetry line thereof.

23. The phase-change memory cell according to claim 18, wherein the upper section has a faceted configuration.

24. The phase-change memory cell according to claim 18, wherein the lower electrode further comprises:

forming a metal compound film disposed in a recess.

25. The phase-change memory cell according to claim 18, wherein the lower electrode further comprises:

a refractory metal compound film disposed in a recess.

26. The phase-change memory cell according to claim 18, wherein the lower electrode further comprises:

a refractory metal compound film in a recess, wherein the refractory metal compound film is selected from tantalum nitride, titanium nitride, tungsten nitride, tanatalum silicon nitride, titanium silicon nitride, and tungsten silicon nitride.

27. The phase-change memory cell according to claim 18, wherein the lower electrode further comprises:

a polysilicon film disposed in a recess.

28. The phase-change memory cell according to claim 18, further comprising:

a phase-change material disposed over the upper section.

29. A process of forming a phase-change memory device comprising:

providing a phase-change memory cell substrate including a lower electrode in a first dielectric film, wherein the lower electrode comprises an upper section and a lower section;

removing a portion of the first dielectric film to cause the upper section to form a prominence;

increasing resistivity in the upper section;

forming a second dielectric film over the upper section;

removing a portion of the second dielectric film to expose an upper surface of the upper section; and

forming a volume of phase-change memory material over the upper section.

30. The process according to claim 29, wherein increasing resistivity further comprises:

treating the upper section under conditions to form at least one of a dielectric husk thereon that forms at least a conductivity gradient taken from a lateral surface of the upper section and tending toward a symmetry line thereof, or that forms an oxidized high resistivity film.